Official Amendment
Serial No: 09/943,078
Attorney Docket MIO 0083 PA

IN THE SPECIFICATION

In accordance with the **REVISED AMENDMENT FORMAT** and waiver of 37 CFR §1.121, as promulgated by order of Stephen Kunin, Deputy Commissioner for Patent Examination Policy, on January 31, 2003,amendments to the specification are made herein by presenting replacement paragraphs marked up to show changes made relative to the immediate prior version, as set out in 37 CFR §1.121(b). No accompanying "clean" version shall be supplied.

Please replace the paragraph on page 9, starting on line 28 with the following:

As illustrated in Fig. 5, a gate oxide layer 50 is grown on the base substrate 12. The gate oxide layer 50 can be grown by thermal oxidation of the base substrate 12, or by other conventional techniques such as chemical vapor deposition (CVD). It will be appreciated that when growing the gate oxide layer 50, the oxide will form on any exposed silicon surface. As such, it may be necessary to remove any undesired oxide that formed as a result of the process. As an example, oxide will grow on the base substrate 12 within the portions of the gate/local interconnect damascene trenches intended to form local connections as illustrated ~~by~~ in the gate/local interconnect damascene trench 46.

B1

Please replace the paragraph on page 11, starting at line 6 with the following:

As illustrated in Fig. 9A, the structure 10 is then planarized using CMP techniques for example. Subsequent to the planarizing process, that portion of the conductive layer 70 that filled the gate/local interconnect damascene trench 44 generally over the gate oxide layer 50 defines the gate conductor 72, and that portion of the conductive layer 70 that filled the gate/local interconnect damascene trench 46 generally over the plug area 66 defines a local interconnect conductor 74.

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